3. (6 pts) **For this question, use the architecture and information on the second page.** Your answers should be optimum in terms of the required clock cycles.

Consider the instruction MAD (memory add opcode) that adds the data in two consecutive effective addresses (EA) in memory and write the result to the next effective address in memory.

**MAD:**

Note: You can ignore ALU control signals. You can overwrite values of the remaining registers.

1. (3 pts) Write the address decoding cycle in RTL and mention the corresponding control signals. It should be performance in one clock cycle.
2. (3 pts) Write the microoperation that write MAD instruction in RTL (after the address decoding cycle) and mention the corresponding control signals (that should be 1) at each clock cycle.